REMARKS

The Office Action mailed June 19, 2002, has been received and reviewed. Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 are currently pending in the referenced application. All pending claims stand rejected. No claim amendments have been made by way of the present communication. Applicant respectfully requests reconsideration of the application in light of the following remarks.

35 U.S.C. § 103(a) Obviousness Rejections

(A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. In order "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." MPEP §2143. Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly sugest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). *See also* MPEP §706.02(j) and §2142.

The Supreme Court has established the standard of patentability to be applied in obviousness rejections in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This

standard has been summarized in MPEP § 2141 into four factual inquiries including "(A) [d]etermining of the scope and contents of the prior art; (B) [a]scertaining the differences between the prior art and the claims in issue; (C) [r]esolving the level of ordinary skill in the pertinent art; and (D) [e]valuating evidence of secondary considerations." It should be noted that, when applying the required patentability standards of Graham, the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "(A) [t]he claimed invention must be considered as a whole; (B) [t]he references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) [t]he references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) [r]easonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). *See also* MPEP § 2141.

(B) Obviousness Rejection Based on U.S. Patent No. 6,854,127 to Pan in view of U.S. Patent No. 6,084,304 to Huang et al.

It is stated at ¶ 3 of the outstanding Office Action that claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,854,127 to Pan (hereinafter the "Pan reference") in view of U.S. Patent No. 6,084,304 to Huang et al. (hereinafter the "Huang reference"). Applicant respectfully submits, however, that the above-stated rejection appears from the outstanding Office Action to actually be based upon the Pan reference in view of U.S. Patent No. 5,955,781 to Joshi et al. (hereinafter the "Joshi reference") rather than in view of the Huang reference. The Huang reference is stated in ¶ 4 of the outstanding Office Action to not be relied upon but considered pertinent to applicant's disclosure. Further, the Joshi reference is specifically referred to throughout the text of the rejection. Accordingly, the following remarks address 35 U.S.C. § 103(a) rejection of the

pending claims based upon the Pan reference in view of the Joshi reference. If this understanding is in error, clarification of the rejection is respectfully requested.

As the Examiner has failed to establish a *prima facie* case of obviousness based upon the Pan reference in view of the Joshi reference, applicant respectfully traverses this rejection, as hereinafter set forth.

For the sake of convenience, the independent claims to which the § 103(a) rejection applies are summarized herein. Independent claim 1 recites a contact for a semiconductor device. The contact comprises a single contact plug extending through a first barrier layer planarized down to a transistor gate member, the single contact plug in electrical communication with an active region on a semiconductor substrate. The contact further comprises an individual contact land disposed atop the single contact plug *and a portion of the first barrier layer*, wherein the contact land is wider than the single contact plug and *is substantially planar* (emphasis added). Further, the contact comprises an upper contact extending through a second barrier layer, the second barrier layer disposed over the first barrier layer, to form an electrical contact with the individual contact land.

Independent claim 3 recites a transistor for the dissipation of electrostatic discharges. The transistor comprises, in part, an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one drain region and the at least one source region on the at least one active area. The transistor further comprises a first barrier layer planarized down to the at least one transistor gate member and substantially covering the at least one thick field oxide area, the at least one active area, and adjacent the at least one transistor gate member. The transistor further comprises at least one drain contact plug and at least one source contact plug, both extending through the first barrier layer, an individual drain contact land disposed atop each of the at least one drain contact plugs *and a portion of the first barrier layer* and an individual source contact land disposed atop each of the at least one source contact

plugs *and a portion of the first barrier layer* (emphasis added). The individual drain contact land is wider than the at least one drain contact plug, the individual source contact land is wider than the at least one source contact plug and *both the individual drain contact land and the individual source contact land are substantially planar* (emphasis added). A second barrier layer is disposed over the first barrier layer, the individual drain contact land and the individual source contact land. At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with at least one of the individual source contact lands. The at least one upper drain contact extends through the second barrier layer, the at least one upper drain contact in electrical communication with at least one of the individual drain contact lands.

Independent claim 19 recites a semiconductor device including at least one contact. The semiconductor device of claim 19 comprises a single contact plug extending through a first barrier layer planarized down to a transistor gate member, the single contact plug being in electrical communication with an active region on a semiconductor substrate. The contact further comprises an individual contact land disposed atop the single contact plug *and a portion of the first barrier layer*, the individual contact land being wider than the single contact plug *and substantially planar* (emphasis added). Further, the contact comprises an upper contact extending through a second barrier layer, the second barrier layer disposed over the first barrier layer, to form an electrical contact with the individual contact land.

Independent claim 21 recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharges. The semiconductor device comprises, in part, an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one drain region and the at least one source region on the at least one active area. The semiconductor device further comprises a first barrier layer planarized down to the at least one transistor gate member and substantially covering the at least one thick

field oxide area, the at least one active area, and adjacent the at least one transistor gate member. The transistor further comprises at least one drain contact plug and at least one source contact plug, both extending through the first barrier layer, an individual drain contact land disposed atop each of the at least one drain contact plugs *and a portion of the first barrier layer* and an individual source contact land disposed atop each of the at least one source contact plugs *and a portion of the first barrier layer* (emphasis added). The individual drain contact land is wider than the at least one drain contact plug and the individual source contact land is wider than the at least one source contact plug. A second barrier layer is disposed over the first barrier layer. At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with at least one of the individual source contact lands. The at least one upper drain contact extends through the second barrier layer, the at least one upper drain contact in electrical communication with at least one of the individual drain contact lands.

It is respectfully submitted that a *prima facie* case of obviousness cannot be made with regard to independent claims 1, 3, 19 and 21 based upon the asserted combination of references as the references, whether taken alone or in combination, fail to teach or suggest each and every element of these claims.

The Pan reference discloses integrated circuitry and methods of forming a contact landing pad on a substrate (Abstract; col. 1, lines 6–7). The integrated circuitry of the Pan reference includes a semiconductor substrate 10 with active contact regions 11 formed therein. A plurality of components 12 are formed in spaced relation on the semiconductor substrate 10, the plurality of components 12 comprising first, second and third gates 13, 14 and 15, respectively (col. 1, line 66–col. 2, line 16). A layer of BPSG 27 is formed outwardly of the gates 13, 14 and 15 and the semiconductor substrate 10. A planarization process, such as chemical mechanical polishing, or the like, is utilized to remove excess BPSG (col. 2, lines 24–28). Contact openings 30 are then etched between the individual components 12 to the underlying active contact regions 11, the openings are filled with polysilicon and a planarization process is performed to remove excess

polysilicon. The planarization process forms an inner silicon plug 41 which spans between at least two of the components 12 (col. 2, lines 30–44). An outer silicide layer or portion 60 is formed outwardly of the semiconductor substrate 10 and over the silicon plugs 41. The outer silicide layer 60 has a first surface 61 which joins with the top surface 42 of the inner silicon plugs 41 (effectively moved inwardly from the reaction of a refractory metal layer and appropriate temperature and pressure conditions). Additionally, the outer silicide layer has an elevationally outer second surface 62 which has a greater surface area than the surface area of the top surface 42 (col. 2, lines 45–59).

It is stated in the outstanding Office Action that the Pan reference discloses "[a]n individual contact land (60) disposed atop said single contact plug *and a portion of said first barrier layer*" (27) (emphasis added). Office Action, ¶ 3. Applicant respectfully submits, however, that the outer silicide layer or portion 60 of the Pan reference, while being disposed atop inner silicon plugs 41, is disposed between at least two of the components 12 and is ***not*** disposed atop a portion of the first barrier layer as asserted and recited in each of independent claims 1, 3, 19 and 21 of the referenced application. *See*, the Pan reference, col. 2, lines 30-59. It is readily apparent from a view of FIG. 6 of the Pan reference that the outer silicide layer is disposed atop silicon plugs 41 and portions of gates 13, 14, 15 but is ***not*** disposed atop BPSG layer 27 as asserted.

Further, it is stated in the outstanding Office Action that the Pan reference discloses a contact land that "is wider than said single contact plug and *is substantially planar*" (emphasis added). Office Action ¶ 3. Applicant respectfully submits, however, that the outer silicide layer or portion 60 of the Pan reference, while being wider than the inner silicon plugs 41, is ***not*** substantially planar as asserted in the Office Action and as recited in each of independent claims 1, 3 and 19 of the referenced application. As stated at col. 2, lines 53 – 59 of the Pan reference, the outer silicide layer 60 has an elevationally outer second surface 62 (the top surface thereof in the orientation of the drawing figures) which has a greater surface area than that of the first surface area 61 (the bottom surface in the orientation of the drawing figures) which joins with the

top surface 42 of the inner silicon plug 41. This is due to the fact that the first surface area 61 and the top surface 42 of the inner silicon plug 41 are effectively moved inwardly from the reaction of the refractory metal layer 50 and the appropriate temperature and pressure conditions. *See*, col. 2, lines 45–59. Thus, portions of the first surface area 61 and the outer second surface 62 are not parallel to one another, particularly in those regions which follow the outline of insulative nitride sidewall spacers 26. Thus, the outer silicide layer 60 is ***not*** planar as asserted in the Office Action and as recited in claims 1, 3 and 19 of the referenced application.

It is respectfully submitted that the limitations of claims 1, 3, 19 and 21 discussed above are also not disclosed by the Joshi reference. In fact, the Joshi reference fails to disclose a contact land at all, let alone one which is disposed atop a portion of a first barrier layer and/or which is substantially planar. Accordingly, it is respectfully submitted that the combination of the Pan and the Joshi reference fails to teach or suggest each of the limitations of independent claims 1, 3, 19 and 21 of the referenced application.

It is further respectfully submitted that a *prima facie* case of obviousness cannot be established based upon the asserted combination of references as there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. As stated above, the Pan reference discloses integrated circuitry and methods of forming a contact landing pad on a substrate. The Joshi reference, on the other hand discloses thermal conductors embedded within a semiconductor for dissipating heat from the semiconductor structure and methods of forming such thermal conductors. There is no suggestion or motivation, either from the references or in the knowledge generally available to one of ordinary skill in the art, which would lead one to examine the thermal conductors of the Joshi reference in order to modify the methods of forming landing pads on a substrate as disclosed in the Pan reference. "Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, **there must be some suggestion for doing so** . . ." *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, `598-99 (Fed. Cir. 1988) (emphasis added). "The mere fact that the prior art may be

modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127 (Fed. Cir. 1984). Absent such a suggestion to make the asserted modification, it is respectfully submitted that the Examiner has used impermissible "hindsight" occasioned by the applicant's teachings to hunt through the prior art for the claimed elements and combine them as claimed. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). It is respectfully submitted that such is not an appropriate basis for determining patentability.

In view of the foregoing, applicant respectfully submits that the cited references fail to establish a *prima facie* case of obviousness of independent claims 1, 3, 19 and 21. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103(a) of claims 1, 3, 19 and 21 based upon the asserted combination of the Pan and Joshi references be withdrawn. Claims 1, 3, 19 and 21 are believed to be in condition for allowance and such favorable action is respectfully requested.

Each of the dependent claims of the present invention is also believed to be in condition for allowance because the independent claims from which they depend are in condition for allowance. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)(dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious). Thus, it is respectfully requested that the obviousness rejections of claims 4 through 6, 9, 10, 22 through 24, 27 and 28 be withdrawn as well.

Each of claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 is believed to be in condition for allowance and such favorable action is respectfully requested.

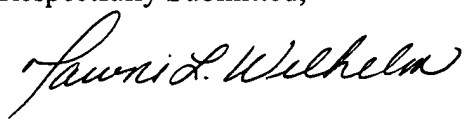
Drawings

Applicant submits herewith, under cover of a separate Letter to the Official Draftsperson, proposed corrections to FIGS. 16, 25 and 29 of the drawings. Specifically, FIG. 16 has been revised to add the reference numeral 144 (twice) with appropriate lead lines; FIG. 25 has been revised to replace one occurrence of reference numeral 186 with reference numeral 188 as the lead line therefore clearly indicates reference to drain contact metallization region 188; and FIG. 29 has been revised to add the reference numeral 104 with appropriate lead line. All proposed corrections have been marked in red. Applicant respectfully requests approval of the corrections to the drawings. Applicant also submits herewith corrected formal drawings, under cover of a separate Transmittal of Formal Drawings. Applicant respectfully requests approval of the corrected formal drawings.

CONCLUSION

Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27 and 28 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact applicant's undersigned attorney.

Respectfully Submitted,



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Date: September 19, 2002

Enclosure: Appendix A – Clean Version of Substitute Specification
Appendix B – Version of Specification with Markings to Show Changes Made

TLW/hlg:dlm

N:\2269\3522.2\Aendment.wpd

FIG. 16

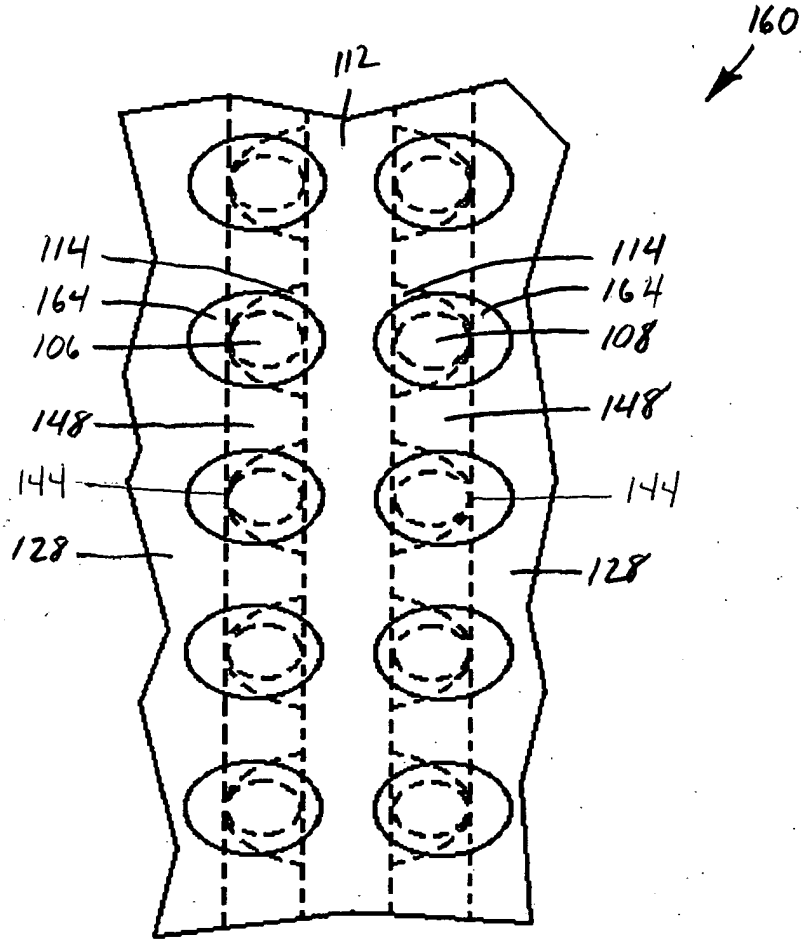


FIG. 25

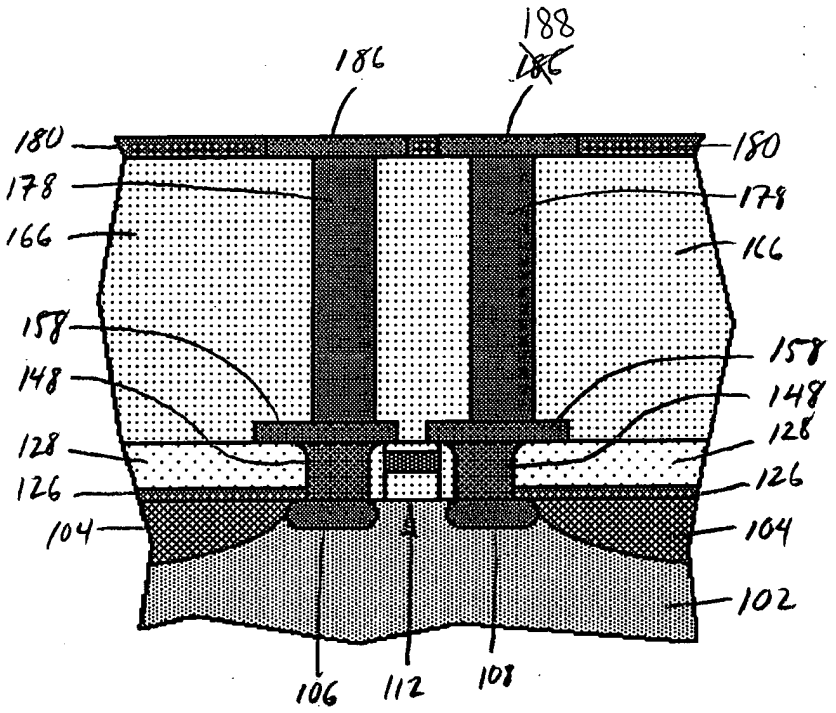
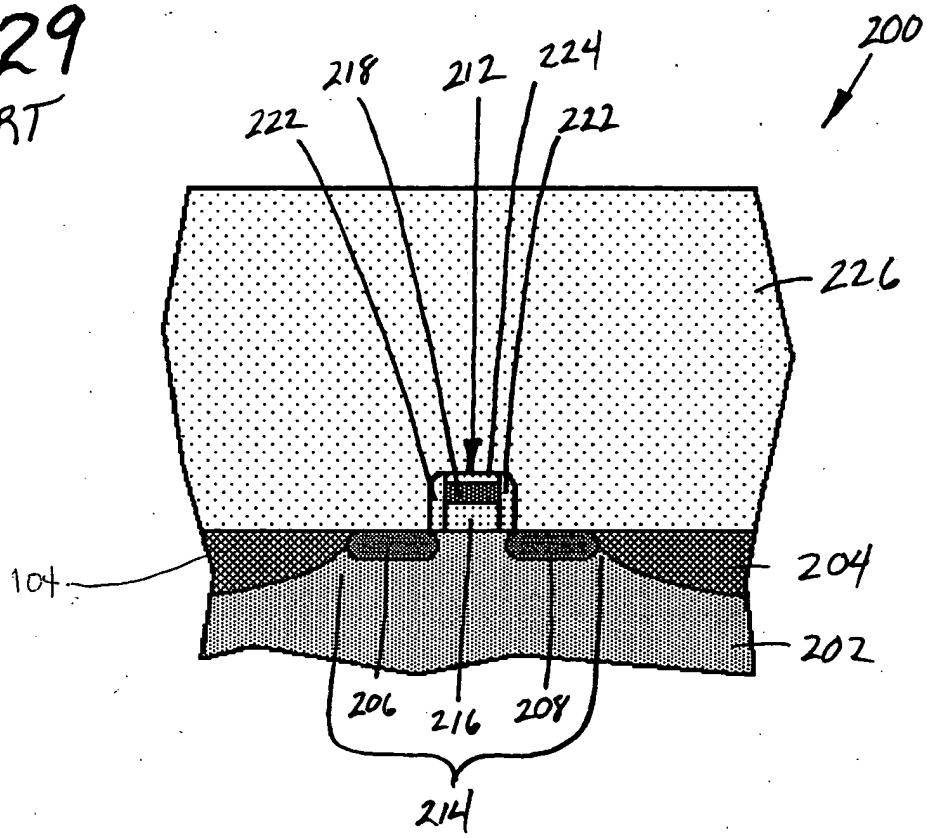


FIG. 29
PRIOR ART



APPENDIX B

VERSION OF SUBSTITUTE SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

(Serial No. 09/146,851)

PATENT
Attorney Docket 3522US(97-1080)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EM548956862US

Date of Deposit with USPS: September 3, 1998

Person Making Deposit: Jared Turner

APPLICATION FOR LETTERS PATENT

for

ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES

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ESD/EOS PROTECTION STRUCTURE FOR INTEGRATED CIRCUIT DEVICES

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: The present invention relates to electrostatic discharge and electrical overstress protection devices and methods of fabricating same. More particularly, the present invention relates to protection devices having charge dissipating structures within the electrostatic discharge and electrical overstress protection devices.

[0002] State of the Art: Electrostatic discharge (hereinafter "ESD") and electrical overstress (hereinafter "EOS") are two common phenomenon that occur during human or mechanical handling of semiconductor integrated circuitry (hereinafter "IC") devices. The input pins to an IC device are highly sensitive to damage from the voltage spike of an ESD, which can reach potentials in excess of hundreds of volts. If a charge of this magnitude is brought into contact with a pin of an IC device, a large flow of current may surge through the IC device. Although this current surge may be of limited energy and duration, it can cause a breakdown of insulating barriers within the IC device (usually gate oxide insulating barriers of an MOS (metal-oxide-semiconductor) IC device). This breakdown of the insulating barriers within an IC can result in permanent damage to the IC device and, once damaged, it is impossible to repair the IC device.

[0003] All pins of a MOS IC device must be provided with protective circuits to prevent such ESD voltages from damaging the insulating barriers (e.g., gate oxide) therein. The most common ESD protection schemes presently used in MOS IC devices rely on the parasitic bipolar transistors associated with an nMOS (n-channel or negative channel metal-oxide-semiconductor) device. These protective circuits are normally placed between the input and output pads (i.e., pin locations) on a semiconductor chip (which contains the IC device) and the transistor gates to which the input and output pads are electrically connected. With such protective circuits under stress conditions, the dominant current conduction path between the protected pin and ground involves the parasitic bipolar transistor of that nMOS device. This parasitic bipolar transistor operates in the snapback region under pin positive with respect

to ground stress events. The dominant failure mechanism found in the nMOS protection device operating in snapback conditions is the onset of second breakdown. Second breakdown is a phenomena that induces thermal runaway in the IC device wherever the reduction of the ESD current is offset by the thermal generation of carriers. Second breakdown is initiated in an IC device under stress, known as electrical overstress or EOS, as a result of self-heating. The peak nMOS device temperature at which second breakdown is initiated is known to increase with the stress current level. The time required for the structure to heat-up to this critical temperature is dependent on the device layout and stress power distributed across the device.

[0004] Higher performance, lower cost, increased miniaturization of components, and greater packaging density of ~~integrated~~ IC devices are ongoing goals of the computer industry. The advantage of increased miniaturization of components include: reduced-bulk electronic equipment, improved reliability by reducing the number of solder or plug connections, lower assembly and packaging costs, and improved circuit performance. In pursuit of increased miniaturization, IC devices have been continually redesigned to achieve ever higher degrees of integration, which has reduced the size of the IC device. However, as the dimensions of the IC devices are reduced, the geometry of the circuit elements have also decreased. In MOS IC devices, the gate oxide thickness has decreased to below 10 nanometers (nm), and breakdown voltages are often less than 10 volts. With decreasing geometries of the circuit elements, the failure susceptibility of IC ~~device~~devices to ESD and EOS increases, and, consequently, providing adequate levels of ESD/EOS protection, has become increasingly more difficult.

[0005] An exemplary method of fabricating an ESD/EOS protection structure (i.e., transistor) is illustrated in FIGs. 29-38. FIG. 29 illustrates a first intermediate structure 200 in the production of a transistor. This first intermediate structure 200 comprises a semiconductor substrate 202, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas 204 and exposed to an implantation processes to form an n-type source region 206 and an n-type drain region 208. A transistor gate member 212 is formed on the surface of the semiconductor substrate 202 residing on a substrate active area 214 spanned between the source region 206 and the drain region 208. The transistor gate member 212

comprises a lower buffer layer 216 separating a gate conducting layer 218 of the transistor gate member 212 from the semiconductor substrate 202. Transistor insulating spacer members 222 are formed on either side of the transistor gate member 212. A cap insulator 224 is formed on the top of the transistor gate member 212. An insulative barrier layer 226 is disposed over the semiconductor substrate 202, the thick field oxide areas 204, the source region 206, the drain region 208, and the transistor gate member 212.

[0006] As shown in FIG. 30, an etch mask 232 is patterned on the surface of the insulative barrier layer 226, such that openings 234 in the first etch mask 232 are located substantially over the source region 206 and the drain region 208. The insulative barrier layer 226 is then etched through openings 234 to form vias 236 which expose a least a portion of the source region 206 and the drain region 208, as shown in FIG. 31. The etch mask 232 is then removed, as shown in FIG. 32. A first conductive material 238 is deposited over the insulative barrier layer 226 to fill the vias 236, as shown in FIG. 33. The first conductive material 238 is planarized, as shown in FIG. 34, to electrically separate the first conductive material 238 within each via 236 (see FIG. 33), thereby forming contacts 242. The planarization is usually performed using a mechanical abrasion process, such as a chemical mechanical planarization (CMP).

[0007] A deposition mask 244 is patterned on the insulative barrier layer 226, having openings 246 over the contacts 242, as shown in FIG. 35. A second conductive material 248 is deposited over the deposition mask 244 to fill the deposition mask openings 246, as shown in FIG. 36. The second conductive material 248 is planarized, as shown in FIG. 37, to electrically separate the second conductive material 248 within each deposition mask opening 246 (see FIG. 35). The planarization is usually performed using a mechanical abrasion, such as a CMP process. The deposition mask 244 is then removed to leave the second conductive material forming a source contact metallization 252 and a drain contact metallization 254, as shown in FIG. 38.

[0008] Although methods as described above are used in the industry, it is becoming more difficult to control the proper alignment of the etch mask 232 for the formation of the contacts 242, as tolerances become more and more stringent. For example, as shown in FIGs.

39 and 40, misalignment of the etch mask 232 can occur. Thus, as shown in FIG. 40, when the insulative barrier layer 226 is etched through the misaligned etch mask 232 to form a first via 256 and a second via 258, the etch forming the first via 256 can destroy a portion of the transistor insulating spacer member 222 and/or the cap insulator 224 to expose the gate conducting layer 218 of the transistor gate member 212. Thus, when a conductive material (not shown) is deposited in the first via 256, the gate conducting layer 218 will short, rendering the transistor ineffectual. Furthermore, the misaligned etch mask 232 can also result in the second via 258 exposing a portion of the field oxide area 204. However, since the etch to form the second via 258 is generally an oxide insulator-type etch, the etch may also etch through the field oxide area 204 to from a third via 262, thereby exposing a portion of the semiconductor substrate 202. Thus, when a conductive material (not shown) is deposited in the second via 258, the conductive material may short with the exposed portion of the semiconductor substrate 202.

[0009] Therefore, it would be desirable to design a transistor which can be fabricated with less sensitivity to misalignment and which has a more efficient charge dissipating structure to handle electrostatic discharge and electrical overstress.

SUMMARY OF THE INVENTION

[0010] The present invention relates methods of forming ~~an~~ electrostatic discharge and electrical overstress protection devices for integrated circuits and devices so formed. The protection devices comprise at least one transistor which includes a shared electrical contact within source regions and within drain regions for more efficient dissipation of an electrostatic discharge which, in turn, reduces the incidence of electrical overstress. The protection devices further include contact plugs and contact landing pads which ~~renders~~render the fabrication of such devices less sensitive to alignment constraint in the formation of contacts for the protection device.

[0011] An exemplary method of fabrication of the transistor of the present application comprises forming an intermediate structure, including a semiconductor substrate, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas

and exposed to n-type implantation processes to form a source region and a drain region. A transistor gate member is formed on the surface of the semiconductor substrate residing on a substrate active area spanned between the source region and the drain region. The transistor gate member comprises a lower buffer layer separating the gate conducting layer of the transistor gate member from the semiconductor substrate. Transistor insulating spacer members, preferably silicon dioxide, are formed on either side of the transistor gate member and a cap insulator is formed on the top of the transistor gate member.

[0012] A first barrier layer, preferably tetraethyl orthosilicate ~~TEOS~~ (TEOS), is disposed over the semiconductor substrate, the thick field oxide areas, the source region, the drain region, and the transistor gate member. A second barrier layer (preferably made of borophosphosilicate glass ~~BPSG~~ (BPSG), borosilicate glass ~~BSG~~(BSG), phosphosilicate glass ~~PSG~~ (PSG), or the like) is deposited over the first barrier layer. It is, of course, understood that a single barrier layer could be employed. However, a typical barrier configuration is a layer of TEOS over the transistor gate member and the substrate followed by a BPSG layer over the TEOS layer. The TEOS layer is applied to prevent dopant migration. The BPSG layer contains boron and phosphorus which can migrate into the source and drain regions formed on the substrate during inherent device fabrication heating steps. This migration of boron and phosphorus can change the dopant concentrations in the source and drain regions, which can adversely affect the performance of the transistor gate member.

[0013] The second barrier layer is then planarized down to the transistor gate member. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process. A first etch mask is patterned on the surface of the planarized second barrier layer, such that openings in the first etch mask are located substantially over the source region and the drain region. The first etch mask openings may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions or drain regions, respectively. The second barrier layer and first barrier layer are then etched to form first vias which expose at least a portion of the source region and the drain region, and the first etch mask is removed. The exposure of the transistor gate member and the etching of such a shallow second barrier

layer and first barrier layer ~~allows~~allow for easy alignment of the first etch mask which, of course, virtually eliminates the possibility of etching through the insulating material of the transistor gate member to expose and short the gate conducting layer within the transistor gate member. A first conductive material is deposited to fill the first vias. The first conductive material is then planarized to isolate the first conductive material within the first vias, thereby forming contact plugs.

[0014] Although any shape of openings in the first etch mask can be used, such as individual openings for each source and drain region, it is preferred that a plurality of ~~the~~ transistors are formed in parallel, such that long, slot-type openings in the first etch mask can be formed. The long slot-type opening, upon etching, forms long, slot vias which expose multiple source regions or multiple drain regions, respectively. Thus, when the first conductive material is deposited in the first vias, the first conductive material will span multiple source or drain regions and, thereby, dissipate an ESD more efficiently.

[0015] A deposition mask is patterned on the second barrier layer, having openings over the contact plugs. The deposition mask openings may be of any shape or configuration, including, but not limited to, circles, ovals, rectangles, or even long slots extending over several source regions and drain regions, respectively. A second conductive material is deposited over the deposition mask to fill the deposition mask openings. The second conductive material is planarized to electrically separate the second conductive material within each deposition mask opening. The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The deposition mask is then removed to leave the second conductive material forming contact lands which are preferably wider than the contact plugs. Again, it is preferred that the contact lands extend over multiple source or drain regions to assist in the dissipation of an ESD.

[0016] A third barrier layer (preferably made of borophosphosilicate glass ~~BPSG~~ (BPSG), phosphosilicate glass ~~PSG~~(PSG), or the like) is deposited over the second barrier layer and the contact lands, and, optionally, planarized. A second etch mask is patterned on the third barrier layer, wherein the second etch mask includes openings substantially aligned over the contact lands. The third barrier layer is then etched down to the contact lands to form

contact vias. As mentioned above, the contact lands are preferably larger than the contact plugs. The larger contact lands provide a bigger "target" for the etch through the third barrier layer to "hit" the contact lands in the formation of the contact vias. Thus, precise alignment becomes less critical.

[0017] The second etch mask is then removed and a third conductive material is deposited over the third barrier layer to fill the contact vias. The third conductive material is then planarized down to the third barrier layer, such as by a CMP method, to electrically isolate the conductive material within each contact via to form upper contacts. A second deposition mask is patterned on the third barrier layer, having openings over the upper contacts. A fourth conductive material is deposited over the deposition mask to fill the deposition mask openings. The fourth conductive material is planarized to electrically separate the fourth conductive material within each deposition mask opening. The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The second deposition mask is then removed to leave the fourth conductive material, forming a source contact metallization and a drain contact metallization, thereby completing the formation of the bipolar transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

[0019] FIG. 1 is a side cross-sectional view of an intermediate structure in a method of forming an ESD/EOS protection structure according to the present invention;

[0020] FIG. 2 is a top plan view ~~along line 2-2 of FIG. 1~~ illustrating a plurality of intermediate structures;

[0021] FIG. 3 is a side cross-sectional view of the intermediate structure after planarization of a barrier layer according to the present invention;

[0022] FIG. 4 is a side cross-sectional view of a etch mask patterning over the structure of FIG. 3 according to the present invention;

[0023] FIG. 5 is a side cross-sectional view of the structure of FIG. 4 after etching according to the present invention;

[0024] FIG. 6 is a side cross-sectional view of the structure of FIG. 5 after removal of the etch mask according to the present invention;

[0025] FIG. 7 is a top plan view of the structure of FIG. 6, wherein long, slot-type openings are used to form long, slot vias according to the present invention;

[0026] FIG. 8 is a top plan view of the structure of FIG. 6, wherein oval openings over each source and drain region respectively are used to form individual vias according to the present invention;

[0027] FIG. 9 is a side cross-sectional view of the structure of FIG. 6 after the deposition of a first conductive material to contact source and drain regions according to the present invention;

[0028] FIG. 10 is a side cross-sectional view of the structure of FIG. 9 after the planarization of the first conductive material according to the present invention;

[0029] FIG. 11 is a side cross-sectional view of the structure of FIG. 10 after the patterning of a deposition mask according to the present invention;

[0030] FIG. 12 is a side cross-sectional view of the structure of FIG. 11 after the deposition on a second conductive material according to the present invention;

[0031] FIG. 13 is a side cross-sectional view of the structure of FIG. 12 after the planarization of the second conductive material according to the present invention;

[0032] FIG. 14 is a side cross-sectional view of the structure of FIG. 13 after the removal of the deposition mask according to the present invention;

[0033] FIG. 15 is a top plan view of the structure of FIG. 14, wherein long, slot-type openings are used to form long contact lands ~~form~~from the second conductive material according to the present invention;

[0034] FIG. 16 is a top plan view of the structure of FIG. 14, wherein oval openings are used to form multiple, individual contact lands according to the present invention;

[0035] FIG. 17 is a side cross-sectional view of the structure of FIG. 14 after the deposition of a third barrier layer according to the present invention;

[0036] FIG. 18 is a side cross-sectional view of the structure of FIG. 17 after the patterning of a second etch mask according to the present invention;

[0037] FIG. 19 is a side cross-sectional view of the structure of FIG. 18 after the etching of the third barrier layer to form contact vias according to the present invention;

[0038] FIG. 20 is a side cross-sectional view of the structure of FIG. 19 after the removal of the second etch mask according to the present invention;

[0039] FIG. 21 is a side cross-sectional view of the structure of FIG. 20 after the deposition of a third conductive material to fill the contact vias according to the present invention;

[0040] FIG. 22 is a side cross-sectional view of the structure of FIG. 21 after the planarization of the third conductive material according to the present invention;

[0041] FIG. 23 is a side cross-sectional view of the structure of FIG. 22 after the patterning of a deposition mask according to the present invention;

[0042] FIG. 24 is a side cross-sectional view of the structure of FIG. 23 after the deposition of a fourth conductive material according to the present invention;

[0043] FIG. 25 is a side cross-sectional view of the structure of FIG. 24 after the planarization of the fourth conductive material according to the present invention;

[0044] FIG. 26 is a side cross-sectional view of the structure of FIG. 25 after the removal of the second deposition mask to form a source contact metallization and a drain contact metallization according to the present invention;

[0045] FIG. 27 is a top ~~plane~~plan view of the source contact metallization and the drain contact metallization according to the present invention;

[0046] FIG. 28 is a schematic of the ESD/EOS protection structure between the drain input pad and integrated circuitry to be protected according to the present invention;

[0047] FIGs. 29-38 are side cross-sectional views of an exemplary prior art method of forming a transistor; and

[0048] FIGs. 39-40 are side cross-sectional views of the exemplary prior art method of FIGs. 29-38 for forming a bipolar transistor wherein an etch mask is misaligned during fabrication thereof.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0049] FIGs. 1-28 illustrate various views of techniques according to the present invention for forming ESD/EOS protection structures. It should be understood that the figures presented in conjunction with this description are not meant to be actual cross-sectional views of any particular portion of an actual semiconductor device, but are merely idealized representations which are employed to more clearly and fully depict the process of the invention than would otherwise be possible. Elements common between the figures maintain the same numeric designation.

[0050] FIG. 1 illustrates a first intermediate structure 100 in the production of a transistor. This first intermediate structure 100 comprises a semiconductor substrate 102, such as a lightly doped P-type silicon substrate, which has been oxidized to form thick field oxide areas 104 and exposed to n-type implantation processes to form a source region 106 and a drain region 108. A transistor gate member 112 is formed on the surface of the semiconductor substrate 102 residing on a substrate active area 114 spanned between the source region 106 and the drain region 108. The transistor gate member 112 comprises a lower buffer layer 116, preferably silicon dioxide, separating a gate conducting layer 118 of the transistor gate member 112 from the semiconductor substrate 102. Transistor insulating spacer members 122, preferably silicon dioxide or silicon nitride, are formed on either side of the transistor gate member 112 and a cap insulator 124, also preferably silicon dioxide or silicon nitride, is formed on the top of the transistor gate member 112.

[0051] A first barrier layer 126, preferably tetraethyl orthosilicate ~~—TEOS~~(TEOS), is disposed over the semiconductor substrate 102, the thick field oxide areas 104, the source region 106, the drain region 108, and the transistor gate member 112. A second barrier layer 128 (preferably made of borophosphosilicate glass ~~—BPSG~~(BPSG), borosilicate glass —

~~BSG~~(BSG), phosphosilicate glass ~~—PSG~~(PSG), or the like) is deposited over the first barrier layer 126.

[0052] Generally, ~~the~~a plurality of structures are formed in multiple sets on the semiconductor substrate 102. FIG. 2 illustrates a top view of such a plurality of substrate active areas 114 surrounded by the thick field oxide area 104, wherein the substrate active areas 114 include the source regions 106, the drain regions 108, and the transistor gate member 112 spanning and intersecting the substrate active areas 114, prior to the deposition of the first barrier layer 126 and the second barrier layer 128.

[0053] As shown in FIG. 3, the second barrier layer 128 is then planarized down to the transistor gate member 112. The planarization is preferably performed using a mechanical abrasion, such as a chemical mechanical planarization (CMP) process. As shown in FIG. 4, a first etch mask 132, such as photoresist, is patterned on the surface of the planarized second barrier layer 128, such that openings 134 in the first etch mask 132 are located substantially over the source region 106 and the drain region 108. The etch mask openings 134 may be of any shape or configuration, including but not limited to circles, ovals, rectangles, or even long slots extending over several source regions 106 and drain region 108, respectively. The second barrier layer 128 and first barrier layer 126 are then etched to form first vias 136 to expose at least a portion of the source region 106 and the drain region 108, as shown in FIG. 5. The etch mask 132 is then removed to form a second intermediate structure 140, as shown in FIG. 6.

[0054] FIGs. 7 and 8 illustrate top plan views of the second intermediate structure 140 of FIG. 6, wherein different ~~shape~~shaped openings 134 of the etch mask 132 (see FIG. 5) are utilized. FIG. 7 is the resulting intermediate structure 140 wherein long, slot-type openings ~~were~~are utilized to form long, slot vias 142 which expose multiple source regions 106 and multiple drain regions 108, respectively. FIG. 8 is a resulting intermediate structure 140 wherein oval openings are utilized to form multiple, individual vias 144 which expose individual source regions 106 and individual drain regions 108 (active areas 114, source regions 106, and drain regions 108 are shown in shadow for visual orientation).

[0055] As shown in FIG. 9, a first conductive material 146, such as n-type doped polysilicon, is deposited such that the first vias 136 are filled therewith. The first conductive material 146 is then planarized to isolate the first conductive material 146 within the first vias 136, thereby forming contact plugs 148, as shown in FIG. 10. Preferably, the first vias 136 are formed as long, slot vias 142, as shown in FIG. 7, as the first conductive material 146 in each slot via will span multiple source or drain regions and, thereby, dissipate an ESD more efficiently.

[0056] A deposition mask 152, such as TEOS, is patterned on the second barrier layer 128 having openings 154 over the contact plugs 148, as shown in FIG. 11. The deposition mask openings 152 may be of any shape or configuration, including, but not limited to, circles, ovals, rectangles, or even long slots extending over several source regions 106 and drain region 108, respectively. A second conductive material 156, such as n-doped polysilicon, is deposited over the deposition mask 152 to fill the deposition mask openings 154, as shown in FIG. 12. The second conductive material 156 is planarized, as shown in FIG. 13, to electrically separate the second conductive material 156 within each deposition mask opening 154 (see FIG. 11). The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The deposition mask 152 may be removed (optional) to leave the second conductive material forming contact lands 158 on a third intermediate structure 160, as shown in FIG. 14.

[0057] FIGs. 15 and 16 illustrate top plan views of the third intermediate structure 160 of FIG. 14, wherein different shape openings 154 of the deposition mask 152 (see FIG. 11) were utilized. FIG. 15 is the resulting intermediate structure 160 wherein long, slot-type openings are utilized to form long, contact lands 162 spanned over multiple source regions 106 (shown in shadow) and multiple drain regions 108 (shown in shadow), respectively (active areas 114, transistor gate members 112, and contact plugs 148 (formed in the long, slot vias 142, as shown in FIG. 7) are also shown in shadow for visual orientation). FIG. 16 is the resulting intermediate structure 160 wherein oval openings are utilized to form multiple, individual contact lands 164 atop the contact plugs 148 formed in multiple, individual

vias 144, as shown in FIG. 8 (contact plugs 148, source regions 106, drain regions 108, active areas 114, and gate members 112 shown in shadow for visual orientation).

[0058] A third barrier layer 166 (preferably made of borophosphosilicate glass — ~~BPSG~~(BPSG), phosphosilicate glass ~~PSG~~(PSG), or the like) is deposited over the second barrier layer 128 and the contact lands 158, and, optionally, planarized, as shown in FIG. 17. A second etch mask 168, such as photoresist, is deposited on the third barrier layer 166, wherein the second etch mask 168 includes ~~opening~~openings 172 substantially aligned over the contact lands 158, as shown in FIG. 18. The third barrier layer 166 is then etched down to the contact lands 158 to form contact vias 174, as shown in FIG. 19, and the second etch mask 168 is then removed, as shown in FIG. 20.

[0059] A third conductive material 176, such as titanium nitride or tungsten, is deposited over the third barrier layer 166 to fill the contact vias 174 (see FIG. 20), as shown in FIG. 21. The third conductive material 176 is then planarized down to the third barrier layer 166, such as by a CMP method, to electrically isolate the conductive material 176 within each contact via 174 to form upper contacts 178, as shown in FIG. 22.

[0060] A second deposition mask 180, such as TEOS, is patterned on the third barrier layer 166, having openings 182 over the upper contacts 178, as shown in FIG. 23. A fourth conductive material 184 is deposited over the deposition mask 180 to fill the deposition mask openings 182, as shown in FIG. 24. The fourth conductive material 184 is planarized, as shown in FIG. 25, to electrically separate the fourth conductive material 184 within each deposition mask opening 182 (see FIG. 23). The planarization is preferably performed using a mechanical abrasion, such as a CMP process. The second deposition mask 180 is then removed to leave the fourth conductive material forming source contact metallization 186 and a drain contact metallization 188 resulting in an ESD/EOS protection structure 190, as shown in FIG. 26.

[0061] FIG. 27 illustrates a top ~~plane~~plan view of the source contact metallization 186 and the drain contact metallization 188. The source contact metallization 186 is in electrical communication with a source plate 194 and the drain contact metallization 188 is in contact with a drain input pad 192. The transistor gate members 112 are connected to a common

electrical contact 196. The transistorgate members 112 and the upper contacts 178 are illustrated for visual orientation, but it is understood that they would not be visible with a top plan view. FIG. 28 illustrates a schematic of the ESD/EOS protection structure between the drain input pad 192 and integrated circuitry 198 to be protected.

[0062] It is, of course, understood that the present invention can be used to form any contact for a semiconductor device, wherein a contact plug (such as contact plug 148) is capped with a contact land (such as contact land 158) in order to make the formation of the contact less sensitive to etch misalignments.

* * * * *

[0063] Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

ABSTRACT

[0064] Apparatus and methods forming electrostatic discharge and electrical overstress protection devices for integrated circuits wherein such devices include shared electrical contact between source regions and between drain regions for more efficient dissipation of an electrostatic discharge. The devices further include contact plugs and contact lands which ~~renders~~render the fabrication of the devices less sensitive to alignment constraint in the formation of contacts for the device.